

Design and Implementation of VLSI Systolic Array Multiplier for DSP Applications

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ABSTRACT— *Multiplication is most commonly used operation in mathematics. Integer multiplication is used commonly in the real world, binary multiplication is the basic multiplication used for the integer multiplication. Systolic algorithms are the efficient algorithms to perform the binary multiplication [1]. Systolic array is an arrangement of processors in an array where data flows synchronously across the array between neighbors, usually with different data flowing in different directions. Each processor at each step takes in data from one or more neighbors (e.g. North and West), processes it and, in the next step, outputs results in the opposite direction (South and East) [2]. The present work is concentrated on developing hardware model for systolic multiplier using VHDL (Very High Speed Integrated Circuits Hardware Description Language) as a platform. The design is simulated using modelsim simulator and synthesized on Spartan 3 FPGA board.*

Key Words: Systolic Array, Parallel Processing, Xilinx, FPGA, VHDL.

I. INTRODUCTION

The paper briefs about the method to verify appropriate program execution. In order to achieve the high speed and low power demand in DSP applications, parallel array multipliers are widely used. In DSP applications, most of the power is consumed by the multipliers. Hence, low power multipliers must be designed in order to reduce the power dissipation in DSP applications [3]. Systolic algorithm is the form of pipelining, sometimes in more than one dimension. In this algorithm data flows from a memory in a rhythmic

fashion, passing through many processing elements before it returns to memory. H. T. Kung and Charles Leiserson were the first to publish a paper on systolic arrays in 1978, and coined the name, which refers to the “pumping action” of the heart. What can a systolic array do? This question is very important, and the answer is that it is every Sequential algorithm that can be transformed to a parallel version suitable for running on array processors that execute operations in the so-called systolic manner, and systolic array is one of solutions to the need for a highly parallel computational power. Due to the use of matrix-multiplication algorithm in wide fields such as Digital Signal Processing (DSP), image processing, solutions of differential comparison, non-numeric application, and complex arithmetic operations, we shall design a 4-bit systolic array that designed and implements.

VHDL finds many applications because of its very high speed integrated circuit. It is a hardware description language and program can be loaded into the chip and can be used by tool user [5]. As the language supports flexible design methodology, it can be used to define complex electronic systems. Common language can be used to describe the library components [6]. Because of its unique feature, VHDL is used to design N-bit binary multiplier. The program in VHDL provides the scope for multiplication of two N-bit binary numbers by including the user defined package.

II. PURPOSE OF IMPLIMENTATION

The purpose of this implementation is to efficiently resolve a wide spectrum of computational problems by designing and implementing the systolic array architecture on FPGA [3]. Designers search for high performance and flexible architectures; so this paper introduces one of the most efficient

ways to meeting them. The systolic array combines different properties that are seldom found together. These properties are

- 1) Flexible hardware and software (i.e. FPGA technology).
- 2) Spatial and temporal parallelism (i.e. systolic array Architecture).
- 3) Easily scalable architecture.
- 4) High degree of pipelining.

The paper is organized as follows. Section I says about the introduction. Section II deals with purpose of implementation. Section III deals with design methodology. Section IV deals with VHDL implementation of Systolic Multiplier. Section V summarizes the experimental results obtained, while section VI presents the conclusions of the work.

III. DESIGN METHDOLOGY

In systolic multiplication, to carry out the multiplication and get the final product following steps should be followed

1. The multiplicand and multiplier are arranged in the form of array as shown in the Fig. (1).
2. Each bit of multiplicand is multiplied with each bit of multiplier to get the partial products.
3. The partial products of the same column are added along with carry generated.
4. So the resulted output by adding partial products and the carry is the final product of the two binary numbers.

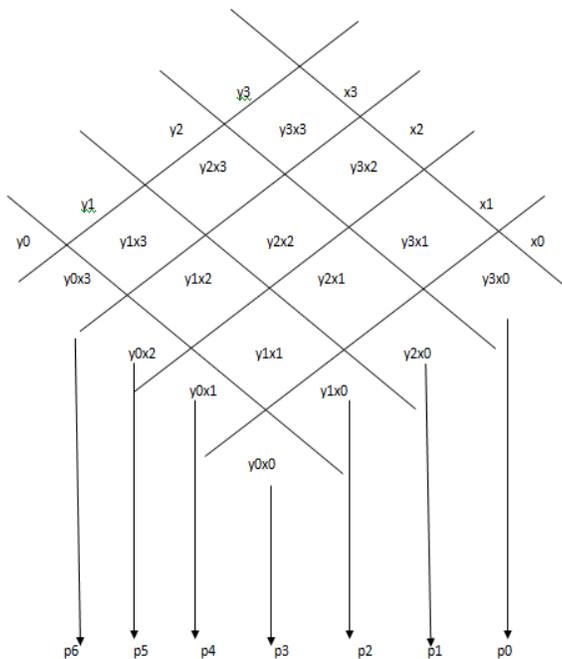


Fig. (1): Methodology of systolic multiplication

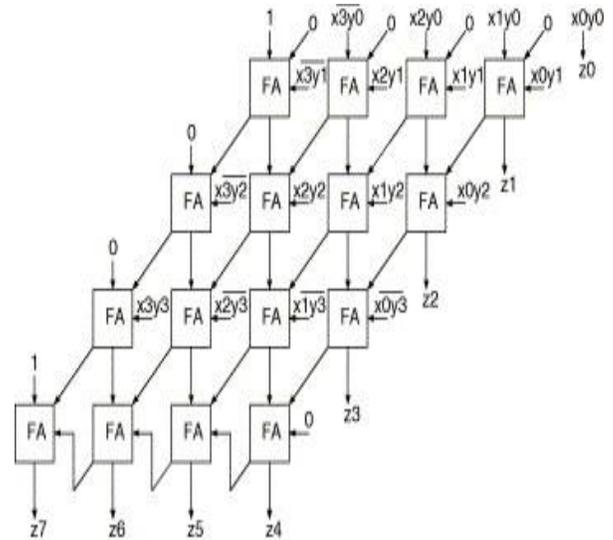
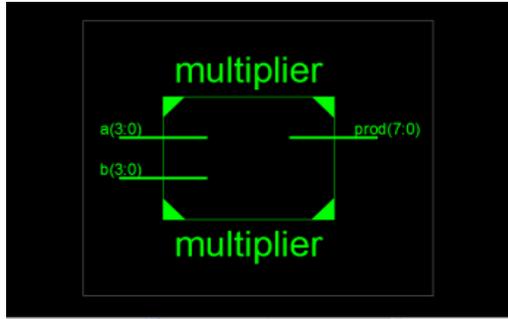


Fig. (2): Block diagram of 4 bit systolic Multiplier

Figure 2 shows the functional units of the 4 bit Systolic Multiplier. Each unit is an independent processing unit. These units share information with their neighbors, after performing the needed operations on the data. Each box in the Fig.(2) represents a full adder. Inputs are vector X and Y are ANDed and the AND outputs are fed as input to full adder, which gives rise to two outputs. One is the actual multiplied output vector Z and another one is the carry generated from the addition of the AND output, which is further used by other full adders. In this way computation takes place simultaneously in the rows and columns. All the inputs are applied simultaneously, therefore registers are not required. Availability of inputs at the start of the computation and the systolic array structure helps the multiplier to perform faster compared to other multipliers.

IV. IMPLEMENTATION

The programming environment for implementing the circuit is based on VHDL. In our implementation Systolic Array Multiplier is designed for 4 bits using structural and behavioral styles and is implemented, tested on the Spartan-3 FPGA board. Obtained results are accurate and error free. In structural modeling, multiplier is divided into 3 sections i.e. upper, middle and lower sections. Where, all the three sections operate on the data simultaneously. Full adder and AND gates are basic building blocks of the multiplier. Each section has 4 full adders and associated AND gates. The entity part or the peripheral view of the multiplier is given in Fig. 3



Fig(3): Entity view of multiplier[]

The behavioral description is written and implemented based on behavior of the Systolic Array multiplier. A timing analysis tool is then applied to the object module to determine maximum operating speed. If algorithms are time consuming then the efficiency of multiplier decreases because, in recent days the efficiency is measured not only with the accuracy but also with the speed. As FPGA is purely hardware circuit, the time taken by it to execute the algorithm is much less [5, 6]. Thus, the Systolic multiplication algorithm implemented on FPGA works faster than any other multiplication technique.

V.DEVICE UTILIZATION SUMMARY

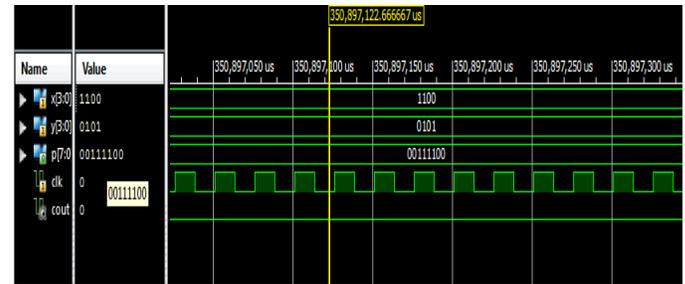
Sl.No	Specifications	Consumed	Total	Percent
1	Number of slices	15	768	1%
2	Number of 4 input LUTs	27	1536	1%
3	Number of bonded IOBs	16	124	12%
4	Global clocks	0	8	0%
5	Power consumption	25mw		

Table 1.

Sl.No	Specifications	Consumed	Total	Percent
1	Number of slices	16	768	2%
2	Number of 4 input LUTs	28	1536	1%
3	Number of bonded IOBs	17	124	13%
4	Global clocks	1	8	12%
5	Power consumption	34mw		

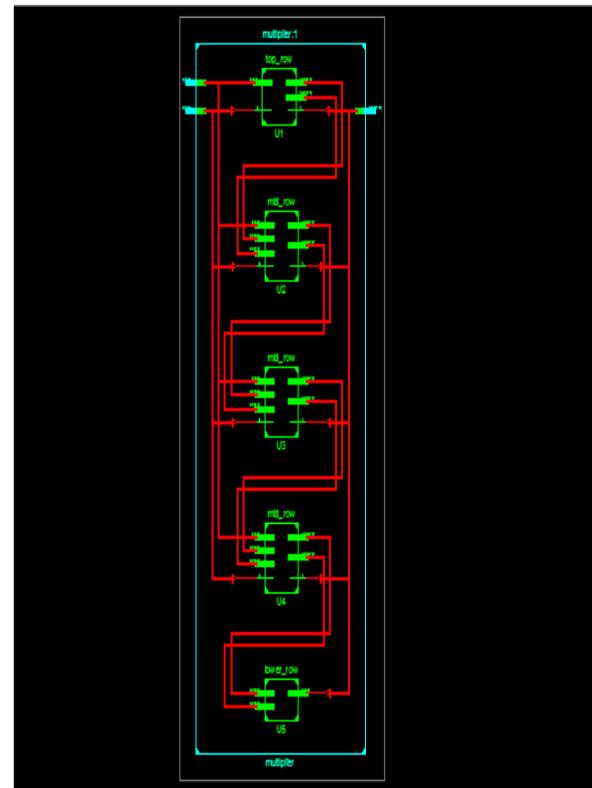
Table 2.

Table 1 and Table 2 shows the device utilization summary obtained from the synthesis report of structural and behavioral modeling respectively. By analyzing the synthesis results there is drastic reduction of resources of FPGA when modeled with two different styles and power consumption is also reduced to a greater extent. Because of this implementation, system requires very less space while designing hardware and eliminates the complexity in hardware design.

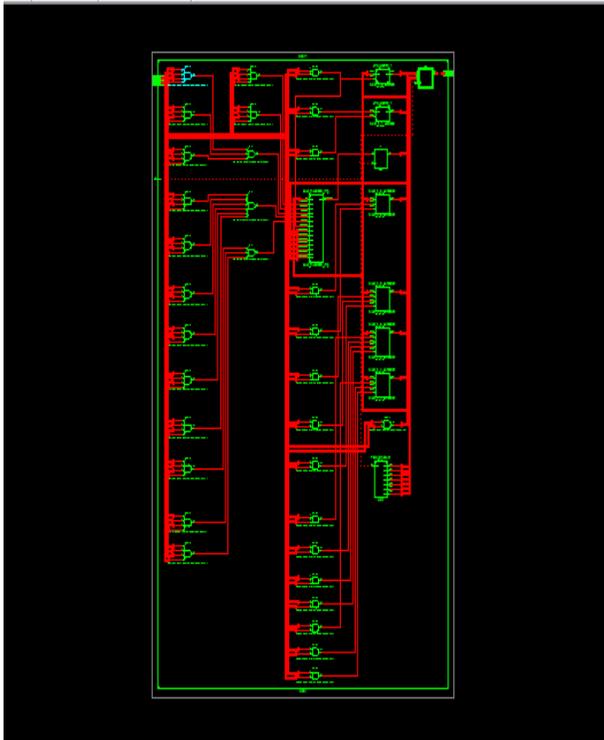


Fig(4): Entity view of multiplier

Simulation results are as shown in the Fig. 4 for inputs 1100 and 0101 and the output obtained is 00111100. Fig. 5 and Fig.6 shows the RTL schematic of the 4 bit Systolic Array Multiplier obtained by using structural and behavioral style of modeling



Fig(5): RTL schematic for structural style of modeling



Fig(6):RTL schematic for behavioral style of modeling

VII. CONCLUSION

Thus the design of 4 bit Systolic Array Multiplier working with frequency of 211.035 MHz and the proposed design was optimized using structural style compared with behavioral style. The designed circuit has been implemented on FPGA and simulated using Isim simulator version 13.1d simulation software and the results are up to the mark. Again, using Xilinx XST we have synthesized the design on Spartan 3s400pq208 effectively. By implementing such designs in VHDL one easily understands the behavior of designing aspects effectively. If this prototype is implemented in real time then there will n number of advantages benefited to the mankind.

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