

New Approach to Reduce Energy Consumption in Six Transistors SRAM

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Abstract— This paper presents the technique used to reduce the power dissipation in 6T SRAM. Normally there is a power loss in charging and discharging the bit line during reading and writing. This power loss is drastically reduced with the use of additional adiabatic circuit. Simulation of the circuit is done using HSPICE in 65nm technology. This circuit also preserve power during writing phase also.

Keywords— SRAM, power dissipation, stability, low power.

I. Introduction

The low cost consumer electronic devices (cell phone with camera, notepad, hand held low cost computing devices etc.) we enjoy today is the direct impact of much phenomenal development of the VLSI technology. As in late 1970s Moore stated a law that in every eighteen month the number of transistor in the chip becomes double. Therefore, to meet the requirement of the portable appliances various low power techniques had been used [I].

Low power design plays a significant role in high-performance IC leads to circuit designs with high clock frequencies. Due to the increase in clock frequency, there is a proportional increase in power dissipation. Moreover, for most portable systems, the IC (Integrated Circuit) components consume a significant portion of the total system power [II].

The dynamic power consumption equation [III]:

$$P_{Dynamic} = f \cdot C_{interconnect} \cdot V_{dd}^2$$

Where, f is the frequency of operation

$C_{interconnect}$ is the interconnect capacitance

V_{dd} is the supply voltage.

Clearly it can be seen that for every VLSI circuit there is dynamic power dissipation due to the operating frequency, operating voltage and the interconnected capacitance.

In static random access memory (SRAM) also there is dynamic power dissipation, which can be reduced by using several technique. In [IV] it is found that about 70% of the total power is lost while reading and writing into the cell. In six transistors SRAM there are double ended reading is done through two bitlines. The two bitlines are used to obtain the stability in reading and to obtain high signal to noise ratio.

In 1995 D. Someshekar et.al. [V] Says that there is about 85% of the power reduction is obtain by using adiabatic principle. They do not use the extra precharge circuitry. But now there is a scope of improvement in SRAM with respect to energy saving.

Tzartzanis et.al [VI] proposed a new energy recovery latch based with two phase resonant clock driver. It is claimed that the energy-recovery SRAM energy recovery resulted in

significant energy savings (e.g. 59% to 76%) for the different 0.5 μ m SRAM parts at 200 MHz.

In [VII] J.Kim et.al uses a dummy bit line capacitance with a constant load for each pair of bit lines in order to provide a constant load to the charging source during all the operation cycles including hold cycles. They found that 53% of power is saved as compared to conventional SRAM at 400MHz and 2.5V during write cycle.

Shunji Nakata [VIII] connects the high resistive switch in between SRA and VDD and in between SRAM and ground. This arrangement gives the energy saving during writing operation. The switches are operated in such a manner that while writing, the power supply voltage to the SRAM is gradually changed from ground level to VDD level

II. Conventional 6T SRAM

In this section the brief revision on the conventional 6T SRAM is focused. As it seen that the operation of SRAM is divided into three modes that is hold mode, write mode and read mode. The fig 1 shows the circuit diagram for 6T SRAM. There is two cross coupled inverter connected back to back each other. The inverter is made up of two transistors MP1 and MN1. Similarly another inverter is made by the combination of NMOS MN2 and PMOS MP2. The output of one inverter is connected to the input of other inverter.

There are two access transistors AN1 and AN2 both are NMOS type. The source terminals of both the inverter are connected to the output of each inverter. The drain terminal is connected to the bitline and compliment of the bitline. The gate terminal of the access transistor is connected to a signal called as word line (WL). The word line will decide whether the SRAM is in hold mode or in read/write mode. If the WL is low the SRAM cell is disconnected from both the bitlines, hence the data present in the cell will be in the hold state. When the WL is high then the SRAM either perform reading operation or writing operation.

The write driver circuit decide whether to read from the SRAM or to write data into the SRAM. When the WE (write enable) signal is high then the data will be write into the SRAM cell. Otherwise reading is done through read amplifier.

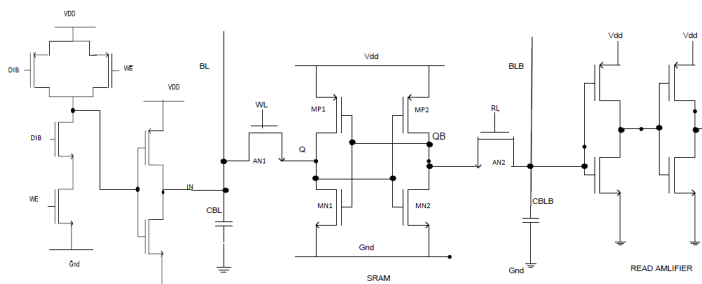


Fig. 1- conventional 6T SRAM with write driver and read amplifier circuit.

The read stability of the cell is obtained by making the transistor MN1 and MN2 greater than the access transistor AN1 and AN2. As it is known that the for reading the data present at the node 'Q' will switch if the NMOS transistor is not greater than the access transistor. The width of the pull up transistor is made smaller as compared to the access transistor and the pull down transistor.

The simulation waveform of the conventional 6T SRAM cell is shown in Fig. 2. The waveform is simulated in HSPICE using Predictive Technology model [IX] in 65nm technology. The waveform shows the writing and reading operation. The voltage used for operating is 1.0V.

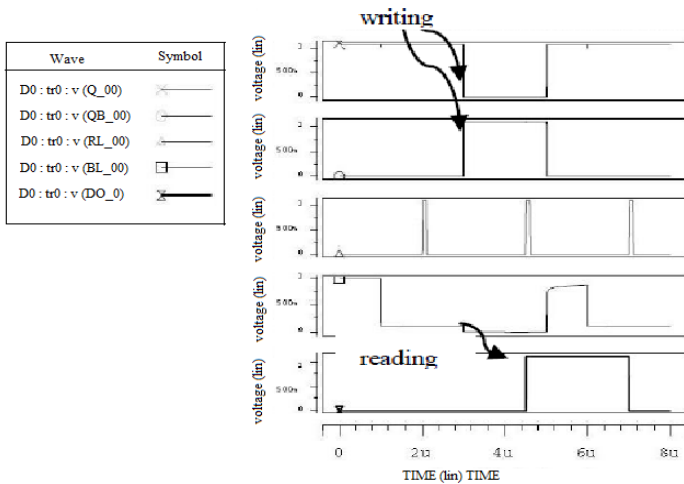


Fig. 2- waveform during write, read and hold operation of conventional 6T SRAM

The energy consumed in the conventional SRAM is $96e-12$ joule. The larger amount of energy is dissipated during writing is about 60% of the total energy dissipated. This energy consumption is reduced by adiabatic technique.

III. Proposed Technique-Adiabatic 6T SRAM

It is seen that there is more power consumption in writing the operation in conventional 6T SRAM cell, hence a new proposed technique is used to reduce the energy consumption during the writing operation.

The proposed circuit for the adiabatic 6T SRAM is shown below in Fig. 3.

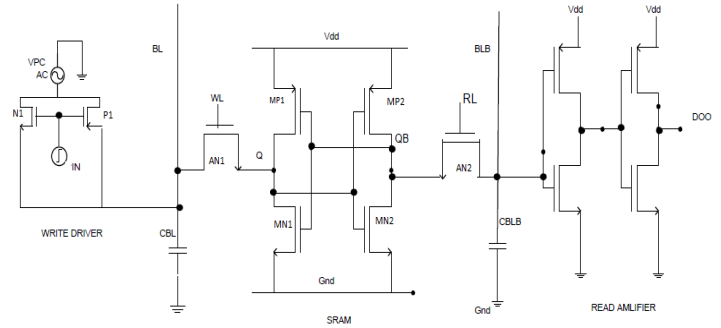


Fig. 3- Adiabatic driver circuit with read amplifier in 6T SRAM

The driver circuit consists of an N and a P MOSFET connected to the capacitance load. When the input signal says 'IN' is low, the capacitance charges to the peak value of the power clock voltage 'Vpc'. When the input signal is high, the charges stored in the capacitance are pumped back to the signal generator.

As we use adiabatic technique there is very less loss of energy. In order to make use of the driver to save energy in bit line, one driver is needed for one bit line.

The energy saved is proportional to:

$$E = \frac{1}{2} \cdot CBL \cdot V^2$$

Where 'CBL' = bit line capacitance and

'V' = bit line voltage

The simulation waveform of the proposed circuit is shown in Fig. 4. The simulation is done in 65nm technology and size of the each transistor is kept in mind to obtain less power dissipation.

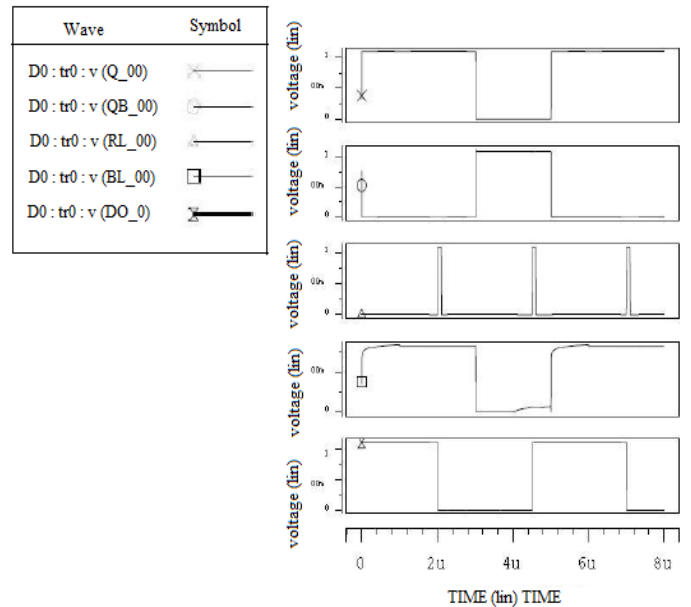
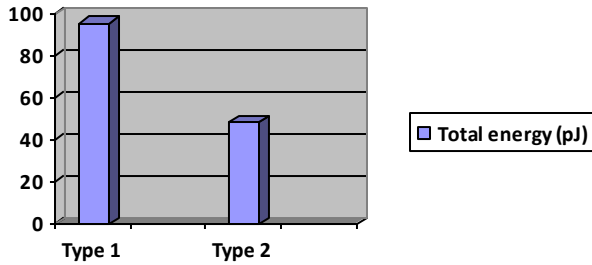


Fig. 4- waveform during write, read and hold operation of proposed 6T SRAM

IV. Results

Here the performance of both the type of SRAM is compared with the help of graph shown below.



Type 1 = Conventional 6T SRAM Type 2 = Adiabatic 6T SRAM

Vertical Column shows the total energy consumption and horizontal axis represent the type of SRAM used. It is clearly seen from the graph that the energy dissipation in conventional SRAM is about 96.06 pJ and the energy consumption in Adiabatic SRAM is 48.54 pJ. It is seen that about 50.54% of energy is saved during writing operation in SRAM cell.

V. Conclusion

With an intension of arriving at a energy efficient SRAM, effort has been put to design an 6T SRAM cell with one bit line for read and one bit line for write along with dual word lines. A simple energy recovery driver along with a larger access transistor connected to the write bit line helps in enhancing the write ability, in addition to saving energy during writing. Read stability has been improved by sizing the pull down transistor connected to the single ended read amplifier.

VI. Acknowledgement

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