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Analysis of Split Gate Technology for Nano-scale Double Gate MOSFET devices

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Abstract: In the present paper we have done a comparative analysis of Dual Gate MOSFET having split gate architecture and conventional Dual Gate MOSFET architecture. Simulations have been performed using SILVACO-ATLAS tool, which shows significant improvement in characteristic of split gate architecture in comparison to the conventional structure. The split gate architecture consist two different materials having different work functions placed laterally to form gate terminal of the MOSFET. This novel gate structure takes advantage of material work function difference in such a way that the threshold voltage near the source is more positive than that near the drain (for n-channel FET, the opposite for p-channel FET), resulting in high output impedance of the device.

Keywords— Dual Gate MOSFET, SILVACO-ATLAS, work functions, threshold voltage, output impedance

I. Introduction

The short channel effects come into existence when the length of gate is reduced to the order of channel depth. The major effects are lack of pinch off and drain current saturation (due to large drain conductance) and large value of leakage current (a shift in threshold voltage, and therefore dependence on drain voltage, due to drain induced barrier lowering (DIBL), and hot-carrier effect) [1].

Dual gate (DG) FET structure is an effective mean to overcome the short-channel effects, due to larger gate area for controlling the channel.[2],[3] The DG-FET, however, does not improve electron transport efficiency [4],[5].

Dual Metal Gate (DMG) Technology was proposed to enhance the electron transport efficiency and further suppress the short channel effects in Double Gate devices [6-10]. This paper presents an analysis of Dual Metal Double Gate (DGDM) MOSFET architecture.

II. Device Structure

The architecture of Dual Gate MOSFET has two gates around the channel. The analysis suggests that a double gate (DG)-MOSFET is promising candidate for high performance operations due to its dual gate architecture which provides better control over the channel region. (Fig.1).

DMDG MOSFET structure consist of two laterally placed gate material in such a way that the gate material having higher work function is placed over the portion of channel which is near to Source and the other insulator material having lower dielectric constant is placed over rest of the portion of channel (Fig.2). This structure results uniform electric field distribution in the channel region and provides screening effect near drain region for better electron transport.

Simulations of DG and DMG architecture have been performed using ATLAS device simulator. The models activated in the simulation comprises of inversion-layer Lombardi constant voltage and temperature (CVT) mobility model, Further, we chose Gummel's method (or the decoupled method), along with Newton's method (or the fully coupled method), to solve the equations included in the CVT model. The simulated results are observed using Tonyplot software package of TCAD tool.

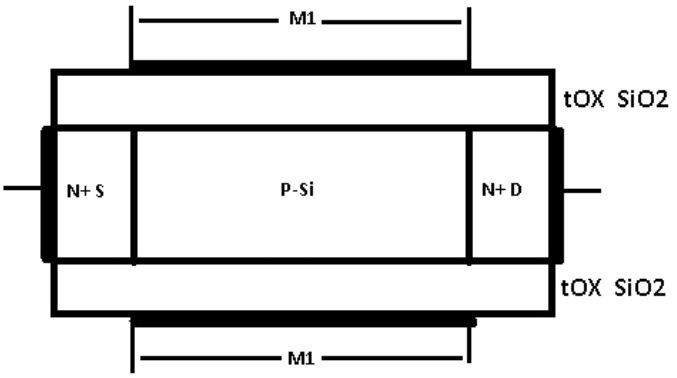

Figure 1. Double Gate MOSFET

I. Results

This dual-material double-gate (DMDG) structure reduces the peak electric field near the drain end, increases the drain breakdown voltage, and reduces the drain conductance and the desired threshold-voltage roll-up for the channel length far below 100 nm (Fig. 2 and Fig. 3)

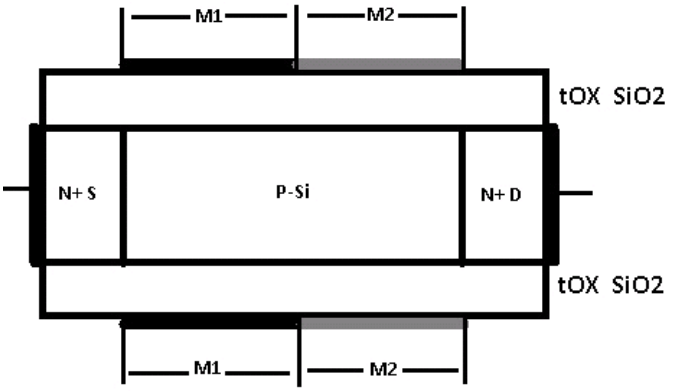

Figure 2. Dual Metal Double Gate MOSFET

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In the DMDG MOSFET, the work-function difference ($q\varphi M1 - q\varphi M2$) between the two gate electrodes M1 and M2 causes an abrupt change in the conduction-band energy at the silicon surface. This generates a step in the potential profile and an

electric-field peak in the channel with a high electric field near the source side. Thus, for the DMDG MOSFET, the electric field at the drain end is reduced, and so the drain conductance (Fig. 4 and Fig. 5).

The change created in electric field distribution by split gate architecture results in relatively slow speed of travelling electron near drain region which further provides lower drain induced barrier lowering effect and better drain conductance as compared with conventional DG MOSFET.

Both the devices (DG MOSFET, DMDG MOSFET) are simulated while maintaining the same off-current Ioff. In order to have an identical Ioff , the DMDG devices have a higher channel doping concentration. Higher doping concentration reduces the surface mobility, and hence, DMDG devices show a lower drain current compared with the DG MOSFET (Fig. 3).

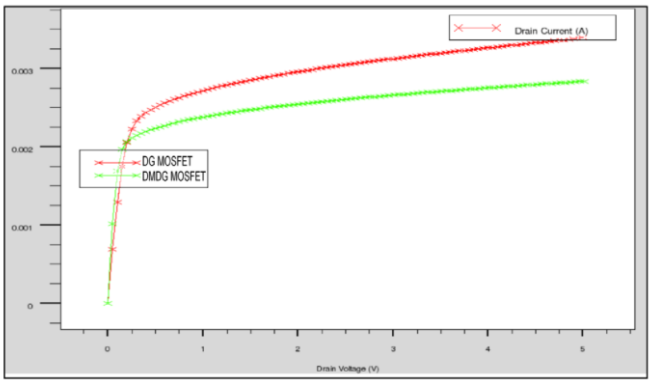

Figure 3. ID-VDS curve for DG MOSFET and DMDG MOSFET

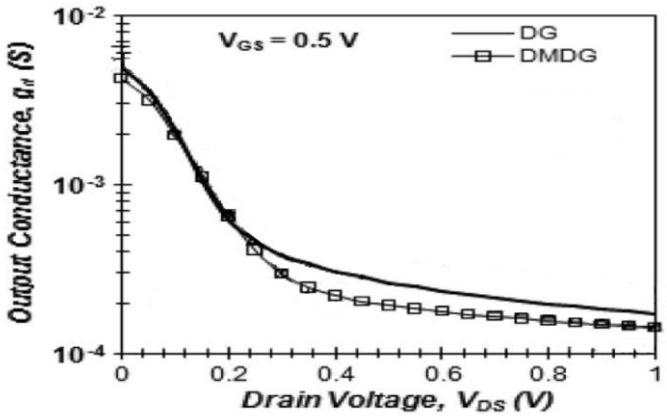

Figure 4. Output conductance- VDS curve comparison

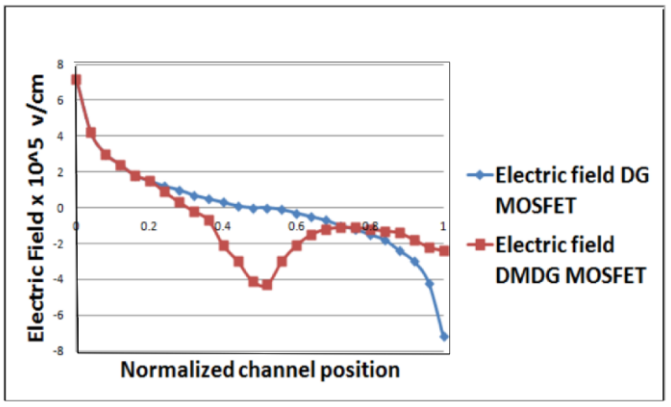

Figure 5. Electric field distribution

IV. Conclusion

A comparative analysis of both the design DMDG MOSFET and DG MOSFET, has been discussed through device simulation along with theoretical support. DMDG structure shows higher output impedance, greater early voltage then conventional DG structure. More ideal output characteristics of DMDG MOSFET makes it suitable candidate specifically for voltage amplification.

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